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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,848	06/27/2006	Mark T. Johnson	GB040001	1326
24737 7590 06/23/2009 PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510			EXAMINER BOLOTIN, DMITRIY	
			ART UNIT 2629	PAPER NUMBER
			MAIL DATE 06/23/2009	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/596,848	Applicant(s) JOHNSON ET AL.	
	Examiner Dmitriy Bolotin	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☒ Claim(s) 16-21 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 June 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

It would be of great assistance to the Office if all incoming papers pertaining to a filed application carried the following items:

1. Application number (checked for accuracy, including series code and serial no.).
2. Group art unit number (copied from most recent Office communication).
3. Filing date.
4. Name of the examiner who prepared the most recent Office action.
5. Title of invention.
6. Confirmation number (See MPEP § 503).

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the **image sensor** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

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of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. **Claim 6** is objected to because of the following informalities: Claim 6 recites "**a display device as claimed**", but does not specify the dependence of claim 6 on any preceding claim, for the purposes of examination claim 6 is treated as if it were dependent on claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

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were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 1 – 8 and 10 – 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereinafter PA) in view of Feurle (US 6,614,704).

As to **claim 1**, PA discloses a display device comprising an array of current-addressed display pixels (pixels 1 of fig. 1) and driver circuitry (shown in fig. 5) for providing pixel drive currents to the pixels of the array (page 10, lines 4 – 8), wherein the driver circuitry comprises a plurality of current drive circuits (each column driver has a current mirror 57 shown in fig. 5, page 9 lines 29 - 30), each having an output transistor arrangement (output transistor 58 of fig. 5),

PA fails to disclose that the output transistor arrangement comprises a plurality of output transistors in parallel, and wherein one or more of the output transistors can be selected in order to provide desired output characteristics.

In the same field of devices used to adjust current level, Feurle discloses a transistor arrangement (element LE of fig. 1) comprises a plurality of output transistors in parallel (transistors T1, T2, and T3 of fig. 1), and wherein one or more of the output

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transistors can be selected in order to provide desired output characteristics (fusible links FL1 and FL2 can be used to set current intensity, col. 4, line 55 - col. 5, line 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify PA by incorporating transistor structure disclosed by Feurle, so as to be able to control current intensity (Feurle, col. 4, lines 63 – 65).

As to **claim 2** (dependent on 1), PA discloses a device, wherein the current drive circuits are at least partially integrated onto the substrate of the array of display pixels (column driver can be formed on the same substrate using same technology as the active matrix, page 5, lines 30 – page 6, line 1).

As to **claim 3** (dependent on 2), PA discloses a device, wherein the display pixels comprise active matrix display pixels (as shown in fig. 2), each comprising a pixel circuit having at least one thin film transistor (drive transistor 22 of fig. 2).

As to **claim 4** (dependent on 3), PA discloses a device, wherein the thin film transistor comprises a polysilicon TFT (active matrix circuits use polysilicon TFTs, page 3, lines 17 – 18), and wherein the output transistors comprise polysilicon TFTs on the same substrate as the display pixels (column driver can be formed on the same substrate using same technology as the active matrix, page 5, lines 30 – page 6, line 1).

As to **claim 5** (dependent on 4), PA discloses a device, wherein the thin film transistor and the output transistors comprise low temperature polysilicon TFTs (majority of active matrix circuits use low temperature polysilicon TFTs, page 3, lines 17 – 18 and column drive made using LPTS technology, page 5, lines 30 – page 6, line 1).

As to **claim 6** (dependent on 1), PA discloses a device, where the output transistors of the current drive circuits are made in the same process as the array of current-addressed display pixels but on a different substrate (control currents can be generated off the substrate, page 9, lines 10 – 14).

As to **claim 7** (dependent on 1), PA discloses a device for driving light emitting display, but fails to disclose that one or more of the output transistors are selected by breaking a fusible link thereby to disconnect the non-selected output transistors.

In the same field of endeavor, Feurle discloses that one or more of the output transistors are selected by breaking a fusible link thereby to disconnect the non-selected output transistors (fusible links FL1 and FL2 can be used to set current intensity, col. 4, line 55 - col. 5, line 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of PA by incorporating fusible link structure disclosed by Feurle, so as to be able to control current intensity (Feurle, col. 4, lines 63 – 65).

As to **claim 8** (dependent on 1), PA discloses a column driving device, but fails to disclose that one or more of the output transistors are selected by electrically connecting them in parallel.

In the same field of endeavor, Feurle discloses that one or more of the output transistors are selected by electrically connecting them in parallel (a fusible link FL1 of fig. 1, between transistors T1 and T2 is not disconnected, col. 4, lines 35 - 55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of PA by incorporating fusible link structure disclosed by Feurle, so as to be able to control current intensity (Feurle, col. 4, lines 63 – 65).

As to **claim 10** (dependent on 8) and **claim 11** (dependent on 10), PA discloses a device for supplying current, but fails to disclose that one of the output transistors is a main output transistor and the others are fine tuning transistors having smaller channel widths than the main output transistor, wherein the channel width/length ratio of each fine tuning transistor is less than 1/25 of the width/length ratio of the main output transistor.

In the same field of endeavor, Feurle discloses that one of the output transistors is a main output transistor (transistor T1 of fig. 1) and the others (transistors T2 and T3 of fig. 1) are fine tuning transistors (fusible links can be interpreted as setting channel width, col. 5, lines 1 – 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of PA by incorporating fusible link structure disclosed by Feurle, so as to be able to control current intensity (Feurle, col. 4, lines 63 – 65).

PA in view of Feurle does not disclose the fine tuning transistors are having smaller channel width/length ratios than the main output transistor, wherein the channel width/length ratio of each fine tuning transistor is less than 1/25 of the width/length ratio

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of the main output transistor. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify PA in view of Feurle so that fine tuning transistors are having smaller channel width/length ratios than the main output transistor in particular less than 1/25 with motivation to introduce a small perturbation to the current through main transistor T1 of Feurle. Such modification would have been an obvious design choice which would have been within a skill of an artisan.

As to **claim 12** (dependent on 8), PA discloses a device for supplying current, but fails to disclose that only one of the output transistors is selected, and the channel width/length ratios of all of the output transistors vary by less than 10%.

In the same field of endeavor, Feurle discloses a device wherein only one of the output transistors is selected (by breaking fusible links FL1 and FL2, transistor T1 is selected, col. 4, lines 35 – 55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify PA by incorporating transistor structure disclosed by Feurle, so as to be able to control current intensity (Feurle, col. 4, lines 63 – 65).

PA in view of Feurle fails to disclose that the channel width/length ratios of all of the output transistors vary by less than 10%. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify PA in view of Feurle so that the channel width/length ratios of all of the output transistors vary by less than 10%, with motivation to modify current through main transistor T1 of Feurle to cover a

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large range of values. Such modification would have been a design choice which would have been within a skill of an artisan.

As to **claim 13** (dependent on 1), PA discloses a device, wherein the current-addressed display pixels comprise electroluminescent display pixels (LED made of electroluminescent material, page 2, lines 14 – 17).

As to **claim 14** (dependent on 13), PA discloses a device, wherein the current-addressed display pixels each comprise an organic LED (Organic light emitting elements, page 2, lines 14 – 17).

As to **claim 15**, PA discloses a method of driving driver circuitry for providing pixel drive currents to the pixels of a display device having an array of current-addressed display pixels (as shown in fig. 1), the driver circuitry comprising a plurality of current drive circuits (each column driver has a current mirror 57 shown in fig. 5, page 9 lines 29 - 30), the method comprising: providing each current drive circuit with an output transistor arrangement (output transistor 58 of fig. 5);

PA fails to disclose a method of tuning driver circuitry, the method comprising: transistor arrangement comprising a plurality of output transistors in parallel; selecting one or more of the output transistors to provide desired output characteristics.

In the same field of devices used to adjust current level, Feurle discloses a method of tuning driver circuitry, the method comprising: transistor arrangement comprising a plurality of output transistors in parallel (element LE of fig. 1); selecting

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one or more of the output transistors to provide desired output characteristics (fusible links FL1 and FL2 can be used to set current intensity, col. 4, line 55 - col. 5, line 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of PA by incorporating transistor structure disclosed by Feurle, so as to be able to control current intensity (Feurle, col. 4, lines 63 – 65).

6. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over PA in view of Feurle and Kubota et al. (US 7,196,699).

As to **claim 9** (dependent on 8), PA in view of Feurle discloses a device for supplying current having output transistors connected to common gate control line, but PA in view of Feurle fails to disclose that one or more of the transistors are selected by further switches which either connect their gate to a common gate control line for the current drive circuit or to a deselect line.

In the same field of endeavor, Kubota discloses a transistor (M16 of fig. 21) selected by further switches (TG and TD of fig. 21) which either connect their gate to a gate control line (line CK of fig. 21) or to a deselect line (GND of fig. 21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of PA in view of Feurle by substituting the fusible link for input control selection of Kubota, so as to provide an alternative way of disconnecting transistors disclosed by Feurle.

Allowable Subject Matter

7. **Claims 16 – 21** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: prior art of record fails to disclose "*a method wherein the selection is performed is based on an analysis of the output characteristics of the display device for a given default selection of the output transistors*"

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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- a. Albert et al. (US 6,825,829) discloses incorporating column driver made using low temperature poly silicon process on the same substrate as active matrix.
- b. Credelle (US 7,046,256) discloses incorporating column driver made using low temperature poly silicon process on the same substrate as active matrix.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dmitriy Bolotin whose telephone number is (571)270-5873. The examiner can normally be reached on Monday-Friday, 8:00 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571)272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. B./
Examiner, Art Unit 2629

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629